Teraptor Designer brings architecture specification and modeling to programmable system design. Teraptor Designer includes languages for processor and system modeling and a comprehensive set of meta-model driven tools for software development, model export, customized RTL code generation (offered as a service), test case generation and verification.

Teraptor Player plays debug-enabled heterogeneous multi-core and multi-component system models. These virtual platforms can be used for various phases of system development and testing.

Teraptor Channels (planned) are ready to use set of components that can be used to kick-start system design using Teraptor Player.

Teraptor helps in creating the next generation of low power and high performance programmable application specific processors and systems. Teraptor can significantly improve productivity and bring scalability to product development processes. Realize business benefits within weeks of adding Teraptor to your strategy.

Benefits for Embedded Software Developers

- Create software before the hardware platform is ready for development.
- Execute a large number of tests in parallel.
- Evaluate software quickly against different system and processor configurations.

Benefits for System Designers

- Integrate processor and system design.
- Achieve superior performance and power usage.
- Enable efficient direct connection architectures.
- Develop hardware and software components in parallel.
- Distribute demos electronically and receive early feedback.
- Simulate hardware defects for validating safety critical systems.
- Reduce time to market; target higher price points.
- Quickly generate product variants for multiple markets.

Benefits for Processor Designers

- A single concise formal specification of processor architecture.
- Enables the creation of configurable processors.
- Reduced time and cost of creating software developer tools.
- Simplified development of application specific processors.
- Automated processor verification.
- Limited circulation of confidential processor architectures.
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